CMOS Current Attenuator for Electrochemical Sensing Applications

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***Abstract*—A new CMOS current attenuator circuit is designed and demonstrated. The purpose of this circuit is to attenuate steady state current in conjunction with CMOS ADC readout circuits for electrochemical sensing applications. The circuit has been fabricated in a 5V AMS CMOS process. Salient features include: (1) bi-directional input current range from 25 nA to 300 nA; (2) current attenuation of 55 dB; (3) non-linearity around 2 % over the entire input current range; (4) output DC offset current of around 200 pA; (5) power consumption around 0.35 mW.**

Keywords—Nanoscaleelectrodes, Microscaleelectrodes, Current attenuator, electrochemical sensing, current mirror

I. INTRODUCTION

Microscale and nanoscale electrodes find widespread use as sensing elements in electrochemical sensing applications [1]. Following advances in microfabrication technology, the state of the art is focused on the integration of these sensors with readout circuits on silicon CMOS substrates. An electrochemical reaction at the surface of an electrode produces a steady state current whose magnitude depends on the surface area of the electrode. This current can range from a few pA to hundreds of nA for nano/micro scale electrodes at typical solution concentrations and this wide dynamic range places a heavy constraint on the design of CMOS sensing circuits. Most CMOS ADC readout circuits are therefore designed for that part of the available current range that is most pertinent to the required application. Currents that fall outside this range must be either amplified or attenuated to operate in conjunction with existing readout circuits. The use of a current amplifier and/or current attenuator as a front-end can increase the effective dynamic range of existing CMOS current sensing circuits. Such amplifiers that amplify current in the sub pA range have been reported in the literature [2]-[5]. However, most report on current attenuators, with many focused on mobile communication applications [6]. Very few CMOS current attenuators have been reported for low frequency applications.

CMOS ADC readout circuits can provide active matrix addressing for electrochemical sensing with arrays of micro/nano-scale electrodes. The individual electrode current to be sensed falls typically between 500 pA and hundreds of nA (this range of current attributed partly to the wide range of electrode area). However, our existing CMOS ADC readout circuit can only sense currents in the range 500 pA - 25 nA. Hence a current attenuator is required in order to use the same readout circuit for electrode currents higher than 25 nA. We propose a current attenuator circuit designed and fabricated in a 5 V 0.35 µm AMS CMOS process that can be used to attenuate a bi-directional steady-state DC input current of amplitude ranging from 25 to 300 nA. The circuit is an open loop architecture which comprises 13 transistors and occupies a footprint of 90×60 µm^2. The current attenuation that can be achieved for the above-stated current range is around 55 dB. An inherent advantage of this circuit, not described further here, is its potential to be used as a current buffer (current mirror).

II. CIRCUIT DESCRIPTION

The current attenuator circuit shown in Fig. 1 consists of a bias circuit block and three distinct stages, with the circuit operating from a 5 V power supply. A detailed description of these three stages follows:

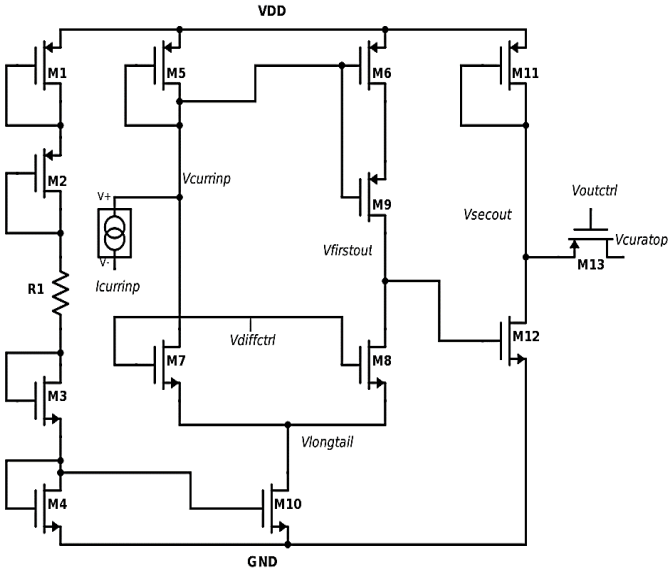

Fig.1. Current attenuator schematic

A. Input current stage

Stage 1 consists of transistors M7 and M5 both biased in saturation. M5 presents a low impedance to the input steady-state current, thereby avoiding significant signal loading. The gates of M7 and M8 are connected to an external DC control voltage labelled "*Vdiffctrl*" in Fig.1. The node labelled "*Vcurrinp*" sources or sinks the input steady-state current "*Icurrinp*".

B. Unbalanced differential stage and bias circuit

This stage consists of transistors M6, M7, M8, M9 and M10. M7 and M8 constitute an un-balanced differential pair of transistors biased in the saturation and linear regions respectively. The inverse relation between current attenuation and the output resistance of M8 is the prime reason behind biasing M8 in the linear region. The aspect ratios of M7 and M8 are identical. Hence, the imbalance in the differential pair is created by M9 being biased in saturation. M9 keeps the drive voltage to the subsequent output stage at a lower level (node labelled "*Vfirstout*" in Fig.1), thereby minimizing the output stage current and power consumption. Also with the introduction of M9, the effect of process variation on the output DC offset current is kept low. The transistor pair M5 and M6 does not form a typical current mirror configuration as M6 is biased in the linear region. M10 sinks a constant current as defined by the bias circuit block. The bias circuit block comprises M1, M2, M3, M4 and R1. R1 is a polysilicon resistor.

C. Output stage

The output stage consists of M11, M12 and M13 all biased in saturation. These transistors were sized to keep the output DC offset current and power consumption at a minimum level. The current attenuation is directly proportional to the ratio of transconductance of transistors M11 and M12, so M11 is sized *slightly* larger than M12. This is because any further increase in the size of M11 intended to produce more current attenuation leads to increased power consumption. On the other hand, any further reduction in the size of M12 leads to an increase in the magnitude of the output DC offset current. The gate control voltage (labelled as "*Voutctrl*" in Fig.1) of M13 is tied to "*Vdiffctrl*" and held at a constant DC level.

This current attenuator circuit has been designed for use in conjunction with a CMOS dual slope ADC readout circuit for electrochemical sensing applications. The output current of the current attenuator is to be sourced into the virtual node of an amplifier that forms a part of the readout circuit. That node is held at a constant DC voltage (midway between the supplies). To cater to this requirement, M13 is used as a bridging transistor whose source and drain terminals are connected to the output stage of the current attenuator ("*Vsecout*" in Fig.1) and a constant DC voltage ("*Vcuratop*" in Fig.1) respectively.

The small signal model for this circuit was developed under the assumption that the input current to the current attenuator is a very low frequency ac current (near steady state with a frequency of the order of several Hz) and the expression for current attenuation derived from the same is:

$$icurrinp/iout = (gm11 \times gds8 \times gm5)/(gm13 \times gm12 \times gm9) \quad (1)$$

gm, gds are MOSFET transconductance and output conductance respectively. From (1), the current attenuation can be observed to be directly proportional to the transconductance of M5, M11 and the conductance of M8; it is also inversely proportional to the transconductance of M13, M12 and M9.

III. Simulation and Experimental Results

A. Experimental set-up for evaluating current attenuation

The test bench comprises:

- An HP 4056 parameter analyzer: Channel 1 was used as a current source to provide steady state current ("*Icurrinp"* in Fig.1) to the current attenuator. Channel 2 was used as a voltage source connected to the node labelled "*Vcuratop*" in Fig.1, which was held at a constant DC voltage of 2.5 V. The output current flows in/out of this voltage source.
- A 5 V Agilent power supply.
- A National Instruments (NI) data acquisition module (DAQ): The control voltages *Vdiffctrl* and *Voutctrl* were generated using two analog output channels of the NI's PCI 6251 DAQ module. Both were held at the same constant DC voltage.

Simulation was carried out by setting up a similar test bench in Cadence Spectre using AMS 0.35µm CMOS process parameters.

B. Test methodology

The input current from channel 1 of the parameter analyzer was swept from 0 to 300 nA and the output current in channel 2 was plotted as a function of input current. Repetitive current sweeps with long integration times (seconds) were performed and the output current plotted after several cycles. A step size of 25 nA was used for the sweep. The conventions used for the current direction are: positive when the channel sources the current and negative when the channel sinks the current.

C. Results

Fig.2. shows the output current plots of the simulation and experimental measurements with *Voutctrl* = *Vdiffctrl* = 2.49 V. This shows that for an input current of 0 nA, the output DC offset current was ~200 pA. For any input current in the specified range, the total output current is the sum of the output DC offset current and the attenuated current component (proportional to the input current). As the input current increases in the nA regime, the output current increases in the pA scale in a linear manner. The percentage of non-linearity and the level of current attenuation over the entire current range are evaluated by measuring the output current values for every 25 nA of input current. This gives 13 data-points in total across the 0 – 300 nA input current range. In this case, the recorded current attenuation for simulation (single simulation run) and experimental results are 58.5 dB and 56.7 dB respectively. Referring to Fig.1, for a fixed *Voutctrl* = *Vdiffctrl* (in this case 2.49 V), an increase in the value of input current from 0 nA (range 0 to +300 nA) increases *Vcurrinp* and the current through M7. This leads to a decrease in the current through M8 as the total current through M10 is constant. However, as M8 is biased in linear region and *vlongtail* ≈ 0 (small signal value of the node labelled *Vlongtail* in Fig.1*)*, a decrease in current through M8 reduces *Vsecout,* which pushes M8 further into the linear region. A reduction in *Vsecout* leads to an increase in the

magnitude of output current. For input currents that flow out of the node labelled *Vcurrinp*, an increase in the input current leads to a decrease in the magnitude of output current.

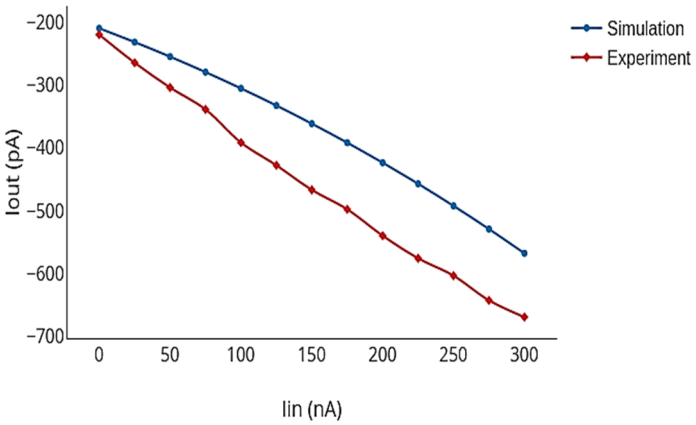

Fig.2. Simulation and experimental results: plot of output current as a function of input current

Fig.3 shows the output current of experiments with *Voutctrl* = *Vdiffctrl* set to 2.48 V and 2.51 V. This is intended to show the effect of control voltages on output DC offset current, current attenuation and non-linearity.

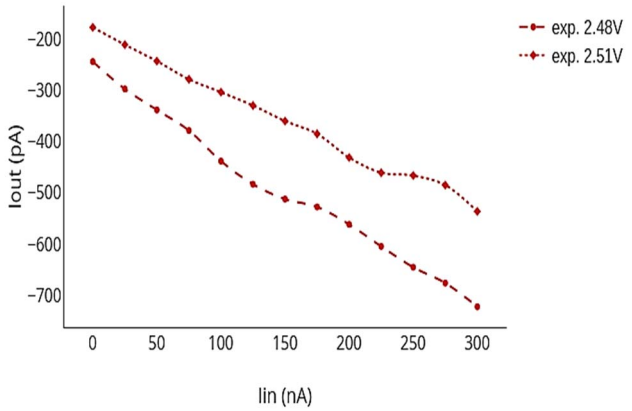

Fig.3. Output current as a function of input current for different control voltages

Referring to Fig.1, with zero input current and an increase in the value of *Vdiffctrl* from a nominal value (e.g. 2.49 V), *Vlongtail* increases to keep the current through M7 at the same level as before. As M8 is biased in the linear region, *Vfirstout* increases to keep the current through M8 at the same level as before. An increase in *Vfirstout* subsequently increases the current through M12, thereby decreasing the output DC offset current through M13. On a similar note, from Fig.3., a decrease in the value of *Vdiffctrl* leads to an increase in the magnitude of the output DC offset current from –200 pA, for *Vdiffctrl* = 2.51 V to around –250 pA for *Vdiffctrl* = 2.48 V. Table I. shows the evaluated experimental results of current attenuation, non-linearity and output DC offset current for different levels of control voltage. Regarding the linearity of the circuit, optimum performance was obtained for *Vdiffctrl* = *Voutctrl* = 2.49 V. By repeatedly sweeping the range of input-current, the output DC offset current was found to vary by 3 % around the nominal value of –224 pA for *Vdiffctrl* = *Voutctrl* = 2.49 V. Static power consumption (V_{DD}*I_{DD}) was measured to be 0.35 mW.

IV. CONCLUSION

A low power current attenuator circuit has been designed and tested in a 5V 0.35µm AMS CMOS process. It functions with single independent DC control voltage, with its intended use being to operate in conjunction with a CMOS ADC readout circuit for sensing steady state currents from electrochemical sensors. Hence the focus was to keep the output DC offset current relatively low in comparison to the full scale current sensing range of an ADC.

Table I. Current attenuator performance parameters

Input-current range: 0 to +300 nA	*Vdiffctrl* =*Voutctrl* = 2.48 V	*Vdiffctrl* =*Voutctrl* = 2.49 V	*Vdiffctrl* =*Voutctrl* = 2.51 V
Output DC offset current (pA)	–250	–224	–183
Current attenuation (dB)	55.9	56.7	59.8
Non-linearity (%)	4.2	2.5	6.5
Input-current range:0 to -300nA			
Current attenuation (dB)	59.3	61.6	65.8
Non-linearity (%)	3.5	2	5.2

A linearity within 2-2.5 % was achieved for the chosen current range. The circuit has the potential to be used in conjunction with CMOS ADC readout circuits to extend their dynamic current sensing range for electrochemical and other sensing applications. Future work will focus on reducing the non-linearity of the circuit, an improved version with closed loop architecture and evaluating the performance with electrochemical sensor.

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